

DECLARATION

As a below-named inventor, I hereby declare that:

My correct residence, post office address and citizenship are stated below next to my name.

I believe myself to be the original, first and sole inventor (if only one name is listed below) or an original and first joint inventor (if more than one name is listed below) of the subject matter which is disclosed and claimed and for which a patent is sought on the invention entitled:

DELAY LOCKED LOOP FOR AN FPGA ARCHITECTURE

The specification of this subject matter:

☐ is attached hereto.

X was filed on March 6, 2000;

was assigned serial No. 09/519,311;

which was amended on _____.

I hereby state that I have reviewed and understand the contents of the above identified patent application, including the claims, as amended by any amendment(s) referred to above. I believe the subject matter claimed in the above-identified application to be new and to be unobvious to persons of ordinary skill in the art in view of the prior art of which I am aware. I further hereby state that the specification of the above identified patent application adequately describes how to make and use the claimed invention, and further that it sets forth the best mode for practicing the invention known to me as of the date that the application was filed. I acknowledge the duty to disclose information which is material to the examination of this application in accordance with 37 C.F.R. §1.56(a).

I hereby claim foreign priority benefits under 35 U.S.C. §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed.

Application No.	Country Filing Date	Priority Claimed
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I hereby claim the benefit under 35 U.S.C. §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in these prior United States application(s) in the manner provided by 35 U.S.C. §112, I acknowledge the duty to disclose material information as defined in 37 C.F.R. §1.56(a) which occurred between the filing date of the prior application(s) and the national or PCT international filing date of this application.

Application No.	Filing Date	Status (Issued, Pending, Abandoned)
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FULL NAME OF INVENTOR 1	FIRST Name	MIDDLE Initial(s)	LAST Name	
	William	C.	Plants	
RESIDENCE AND CITIZENSHIP	City	State or Foreign Country	Country of Citizenship	
	Santa Clara	California	United States of America	
POST OFFICE ADDRESS	Number and Street	City	State or Country	Zip Code
	3295 Brookdale Drive, Apt. #3	Santa Clara	California	95051

FULL NAME OF INVENTOR 2	FIRST Name	MIDDLE Initial(s)	LAST Name	
	Nikhil		Mazumder	
RESIDENCE AND CITIZENSHIP	City	State or Foreign Country	Country of Citizenship	
	San Jose	California	United States of America	
POST OFFICE ADDRESS	Number and Street	City	State or Country	Zip Code
	2865 Ruby View	San Jose	California	94148

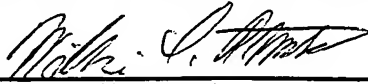


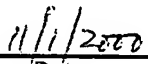
FULL NAME OF INVENTOR 3	FIRST Name	MIDDLE Initial(s)	LAST Name	
	Arunangshu		Kundu	
RESIDENCE AND CITIZENSHIP	City	State or Foreign Country	Country of Citizenship	
	San Jose	California	India	
POST OFFICE ADDRESS	Number and Street	City	State or Country	Zip Code
	4574 Grimsby Rd.	San Jose	California	95130

FULL NAME OF INVENTOR 4	FIRST Name	MIDDLE Initial(s)	LAST Name	
	James		Joseph	
RESIDENCE AND CITIZENSHIP	City	State or Foreign Country	Country of Citizenship	
	Monument	Colorado	United States of America	
POST OFFICE ADDRESS	Number and Street	City	State or Country	Zip Code
	1610 Fawnwood Rd.	Monument	Colorado	80132

FULL NAME OF INVENTOR 5	FIRST Name	MIDDLE Initial(s)	LAST Name	
	Wayne	W.	Wong	
RESIDENCE AND CITIZENSHIP	City	State or Foreign Country	Country of Citizenship	
	Sunnyvale	California	United States of America	
POST OFFICE ADDRESS	Number and Street	City	State or Country	Zip Code
	692 Timberpine Ave	Sunnyvale	California	94086

I further declare that all statements made herein of my own knowledge are true and that all statements made upon information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001

of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

			
Signature of Inventor 1	Date	Signature of Inventor 2	Date
			
Signature of Inventor 3	Date	Signature of Inventor 4	Date
Signature of Inventor 5		Date	

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DELAY LOCKED LOOP FOR AN FPGA ARCHITECTURE

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_____ Signature of Inventor 1	_____ Date	<i>Nikhil Mazumder</i> _____ Signature of Inventor 2	<i>10/12/00</i> _____ Date
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_____ Signature of Inventor 3	_____ Date	_____ Signature of Inventor 4	_____ Date
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Signature of Inventor 3	Date	<i>James Dean Joseph</i> Signature of Inventor 4	<i>October 11, 2000</i> Date
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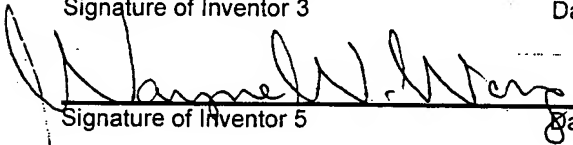
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	10/9/00
Signature of Inventor 5	Date